AMENDMENTS TO THE CLAIMS

1. (Original) An apparatus comprising:

a plurality of logically independent processors;

a system bus; and

a cache control and bus bridge device in communication with the plurality of processors such that it is logically interposed between the processors and the system bus, and wherein the processors and cache control and bus bridge device are disposed in a module form factor such that the apparatus is a drop-in replacement for a standard single-processor module.

2. (Original) The apparatus of claim 1 wherein the processors are IPF processors.

3. (Original) The apparatus of claim 1 wherein a volume of the module form factor is less than or equal to a volume of a standard single-processor module.

4. (Original) The apparatus of claim 3 the standard single-processor module is an ITANIUM 2 module.

5. (Original) The apparatus of claim 1 further comprising a power board and a heat spreader disposed in the module form factor.

6. (Original) The apparatus of claim 5 wherein the processors and cache control and bus bridge device are disposed on a processor board, and wherein the heat spreader is piggybacked onto the power board and the power board is piggybacked onto the processor board.

7. (Original) The apparatus of claim 6 wherein the power board is disposed between the processor board and the heat spreader and wherein a plurality of pedestals on the heat spreader extend through a plurality of holes in the power board thereby contacting one or more of the processors and cache control and bus bridge device such that both the processor board and the power board contact the heat spreader.

8. (Original) The apparatus of claim 7 wherein the pedestals each comprise a variable-gap thermal interface.

9. (Original) The apparatus of claim 8 wherein at least one variable gap thermal interface is a piston and spring thermal interface.

10. (Original) The apparatus of claim 9 wherein at least one variable gap thermal interface has a tolerance of 60 mils.

11. (Original) The apparatus of claim 1 further comprising a power board disposed in the module form factor, wherein the processors and cache control and bus bridge device are disposed on a processor board, and wherein the power board is piggybacked onto the processor board, and wherein a plurality of components of both the power board and processor board are arranged in a complementary skyline and interleaved component fashion.

12. (Original) The apparatus of claim 1 further comprising a power board disposed in the module form factor, wherein the power board utilizes power limiting architecture.

13. (Original) The apparatus of claim 1 further comprising flexible power cable routing within a volume of the form factor.

14. (Original) The apparatus of claim 1 wherein the apparatus is included in a computing device comprising a plurality of similar apparatuses in communication with the system bus.

15. (Original) The apparatus of claim 1 further comprising a power board and a processor board, wherein the processors and cache control and bus bridge device are disposed on the processor board, and wherein the power and processor boards employ micro-vias, accommodated within areas of one or more conductive pads, to provide high current capacity, low impedance paths from surfaces of those boards to a plurality of buried vias and traces in underlying layers of those boards.

16. (Original) A method comprising:

connecting on a local bus a plurality of processors such that the processors are logically independent;

logically interposing between the local bus and a system bus an in-line cache control and bus bridge device;

disposing in a module conforming to a standard single-processor module form factor the plurality of processors, the local bus, and the in-line cache control and bus bridge device; and

operating the plurality of processors and the in-line cache control and bus bridge device such that data input to each of the processors is processed independently and simultaneously.

17. (Original) The method of claim 16 wherein the operating the plurality of processors comprises:

connecting the module to a system board through an interface compatible with a standard single-processor module;

interfacing the system board to a computer system platform;

inputting data to the module from the system board via a system bus

processing the data by a plurality of processors such that each processor processes some of the data independently and simultaneously to the other processors of the plurality; and

receiving by components in the system board processed data from the module via the system bus.

18. (Original) The method of claim 16 wherein the module comprises a piggyback power supply and heat spreader.

19. (Original) The method of claim 18 wherein the power supply comprises a board on which is disposed a plurality of components packed more densely than power components in a power board associated with a single-processor module.

20. (Original) The method of claim 16 further comprising managing a power consumption of the module at a rate equal to or less than a power consumption of a standard single processor module.

21. (Original) The method of claim 20 wherein managing comprises changing a state of the processors from a multi-issue mode to a single-issue mode.

22. (Original) The method of claim 20 wherein managing comprises lowering an operating frequency of the processors while maintaining a performance of each of the processors such that the processors together produce a performance equal to or better than that of a standard single-processor module.

23. (Original) The method of claim 20 wherein the processors together produce a performance of 1.5-2.0 times that of a standard single-processor module.

24. (Original) The method of claim 20 wherein a unit performance per Watt is kept at a maximum for the processors.

25. (Original) The method of claim 16 wherein operating the plurality of processors comprises exchanging data between the processors and a plurality of system components adapted to communicate with a single processor module such that the system components communicate with the plurality of processors as if the system components were communicating with a single-processor module.

26. (Original) The method of claim 16 wherein conforming to a standard single-processor module form factor comprises having a footprint of an area not greater than that of a standard single-processor module and having a volume not greater than that of a standard single-processor module.

27. (Currently Amended) A system comprising:

a plurality of processors mounted onto a ~~at least one~~ processor board;

a power board;

a heat spreader disposed with the plurality of processors and the power board in a first module conforming to a standard single-processor module footprint, wherein the power board is piggybacked with regard to the ~~at least one~~ processor board, wherein the heat spreader is piggybacked with regard to the power board, and wherein the heat spreader thermally contacts the power board and the ~~at least one~~ processor board;

a computer system; and

a system board adapted to communicate with the computer system and comprising an interface adapted to communicate with a standard single-processor module, wherein the first module is coupled to the system board and is in communication with the system board and the computer system.

28. (Original) The system of claim 27 wherein the computer system is a server.

29. (Currently Amended) The system of claim 27 wherein ~~at least one of~~ the processor board ~~boards~~ comprise an in-line cache control and bus bridge device and a fourth level external cache coupled to the in-line cache control and bus bridge device.

30. (Original) The system of claim 27 wherein the first module is a drop-in replacement for a single-processor module.

31. (Original) The system of claim 27 wherein the first module is coupled to the system board by a wedgelock device.

32. (Original) The system of claim 27 further comprising a cooling strap, wherein the cooling strap and the heat spreader comprise a common interface thermal solution.

33. (Original) A multi-processor module comprising:

a plurality of logically parallel processors;

a system bus; and

a cache control and bus bridge device in communication with the plurality of processors such that it is logically interposed between the processors and the system bus, and wherein the processors and cache control and bus bridge device are disposed in a module that is compatible with a single-processor module interface.

34. (Original) The multi-processor module of claim 33 wherein a volume of the module is less than or equal to a volume of a single-processor module.

35. (Original) The multi-processor module of claim 34 further comprising a piggybacked power board and a heat spreader disposed in the module.

36. (Currently Amended) A multi-processor module comprising:

a plurality of processors;

a cache control and bus bridge device that controls access to a common cache by the plurality of processors and electrically isolates the processors from a system bus, said cache control and bus bridge device is adapted to exchange data between the processors and a plurality of system components adapted to communicate with a single processor module such that the system components communicate with the plurality of processors as if the system components were communicating with a single-processor module.

37. (Original) The multi-processor module of claim 36 wherein the module is compatible with a single-processor module interface.

38. (Original) The multi-processor module of claim 36, wherein the processors are IPF processors.

39. (Original) The multi-processor module of claim 36 further comprising a piggybacked power board and a piggybacked heat spreader disposed in the module.

40. (Original) The multi-processor module of claim 36, wherein first module is a drop-in replacement for a single-processor module.

41. (Original) A system comprising:

means for connecting a module to a system board through an interface compatible with a standard single-processor module;

means for interfacing the system board to a computer system platform;

means for inputting data to the module from the system board via a system bus

means for processing the data by a plurality of processors such that each processor processes some of the data independently and simultaneously to the other processors of the plurality; and

means for receiving by components in the system board processed data from the module via the system bus.

42. (Original) The system of claim 41 further comprising means for managing a power consumption of the module at a rate equal to or less than a power consumption of a standard single processor module.

43. (Original) The system of claim 41 further comprising a fourth level external cache included in the module and accessible by the plurality of processors.

44. (Original) The system of claim 41 wherein the means for processing the data by a plurality of processors comprises means for exchanging data between the processors and a plurality of system components adapted to communicate with a single processor module such that the system components communicate with the plurality of processors as if the system components were communicating with a single-processor module.

45. (New) The system of claim 27, wherein said processors are in communication with a cache control and bus bridge device that is interposed between said processors and a system bus.

46. (New) The apparatus of claim 1 further comprising a plurality of multi-processor modules in communication with said system bus.

47. (New) The multi-processor module of claim 33 wherein said cache control and bus bridge device is adapted to exchange data between the processors and a plurality of system components adapted to communicate with a single processor module such that the system components communicate with the plurality of processors as if the system components were communicating with a single-processor module.